

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

PUBLICATION NUMBER : 03034718  
PUBLICATION DATE : 14-02-91

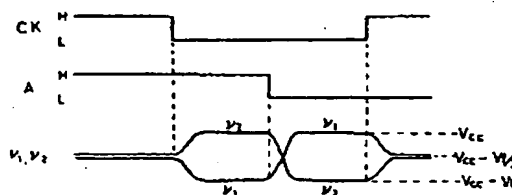
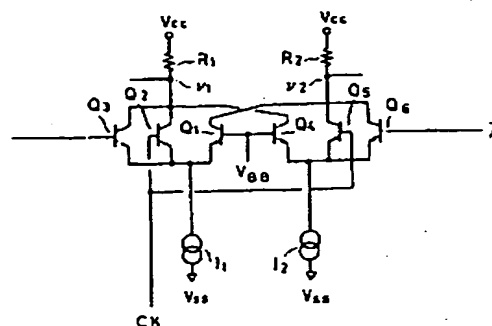
APPLICATION DATE : 30-06-89  
APPLICATION NUMBER : 01169677

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INT.CL. : H03K 3/286 H01L 27/082

TITLE : SEMICONDUCTOR INTEGRATED CIRCUIT



**ABSTRACT :** PURPOSE: To make the lower limit of a power voltage sufficiently small by inputting complementary input signals to the bases of 3rd and 6th bipolar transistors(TRs), applying a clock signal to the bases of 2nd and 5th bipolar TRs, and feeding a reference signal to the bases of 1st and 4th TRs.

CONSTITUTION: The bases of TRs Q<sub>1</sub>, Q<sub>4</sub> are connected in common, a reference voltage V<sub>BB</sub> is applied to the connecting point and a clock CK is inputted to the bases of the TRs Q<sub>2</sub>, Q<sub>5</sub>. Moreover, complementary input signals A, A' are inputted to the bases of TRs Q<sub>3</sub>, Q<sub>6</sub>. When the clock CK is at a high level, a same potential  $V_{CC} - V_1/2$  appears at the nodes v<sub>1</sub>, v<sub>2</sub> and when the clock CK is at a low level, an ECL logic signal appears at the nodes v<sub>1</sub>, v<sub>2</sub> depending on the inputs A, A'. Thus, the transfer of data by the clock without series gating. As a result, a high voltage source V<sub>CC</sub> is made close to a low voltage source V<sub>SS</sub> and the lower limit of the power voltage is sufficiently made small.

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